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INSULATED GATE SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF
[Zetsuen geeto-gata handotai soshi oyobi sono seizo hoho]

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SPECIFICATION /1*

[TITLE OF THE INVENTION]

Insulated Gate Semiconductor Device and Manufacturing Method Thereof

[CLAIMS]

[Claim 1] An insulated gate semiconductor device, characterized by providing

a first semiconductor region of a first conductive type,

a second semiconductor region of a second conductive type formed in a stripe on a surface region of said first semiconductor region,

a third semiconductor region of the first conductive type formed on a surface region of said second semiconductor region, and

a striped gate electrode disposed facing said second semiconductor region between said first semiconductor region and said third semiconductor region,

and disposing said third semiconductor region intermittently along said second semiconductor region.

[Claim 2] The insulated gate semiconductor device according to Claim 1, characterized by providing a bus line connected to one terminal of said gate electrode and to an external electrode, and disposing said third semiconductor region intermittently along said second semiconductor region starting from the vicinity of the connecting portion between said gate electrode and said bus line.

*Claim and paragraph numbers correspond to those in the foreign text.

[Claim 3] The insulated gate semiconductor device according to Claim 2, characterized by said third semiconductor region being of constant width, and disposed such that the length in the direction in which said second semiconductor region extends in a stripe increases as the distance from the vicinity of the connecting portion between said gate electrode and said bus line increases.

[Claim 4] The insulated gate semiconductor device according to Claim 2, characterized by disposing said third semiconductor region such that the area facing said gate electrode increases as the distance from the vicinity of the connecting portion between said gate electrode and said bus line increases.

[Claim 5] The insulated gate semiconductor device according to Claim 2, characterized by disposing said third semiconductor region such that its exposed area increases as the distance from the vicinity of the connecting portion between said gate electrode and said bus line increases.

[Claim 6] The insulated gate semiconductor device according to Claim 2, characterized by said third semiconductor region being of constant width, and disposed such that the gap between said third semiconductor regions decreases as the distance from the vicinity of the connecting portion between said gate electrode and said bus line increases.

[Claim 7] The insulated gate semiconductor device according to

Claim 2, characterized by disposing said third semiconductor region such that the proportion per a specific area occupied by the exposed area of said third semiconductor region lying within the surface of said second semiconductor region increases as the distance from the vicinity of the connecting portion between said gate electrode and said bus line increases.

[Claim 8] An insulated gate semiconductor device, characterized by providing

a first semiconductor region of a first conductive type,

a second semiconductor region of a second conductive type formed in a stripe on a surface region of said first semiconductor region,

a third semiconductor region of the first conductive type formed on a surface region of said second semiconductor region,

a striped gate electrode disposed facing said second semiconductor region between said first semiconductor region and said third semiconductor region, and

a main electrode electrically connected to said second semiconductor region and said third semiconductor region,

and disposing the connecting portion between said second semiconductor region and said main electrode intermittently along said second semiconductor region.

[Claim 9] The insulated gate semiconductor device according to Claim 8, characterized by providing a bus line connected to one terminal of said gate electrode and to an external electrode, and

disposing the connecting portion between said second semiconductor region and said main electrode intermittently along said second semiconductor region starting from the vicinity of the connecting portion between said gate electrode and said bus line.

[Claim 10] The insulated gate semiconductor device according to Claim 9, characterized by disposing the area of the connecting portion between said second semiconductor region and said main electrode so as to decrease as the distance from the vicinity of the connecting portion between said gate electrode and said bus line increases.

[Claim 11] The insulated gate semiconductor device according to Claim 10, characterized by disposing said third semiconductor region intermittently along said second semiconductor region.

[Claim 12] The insulated gate semiconductor device according to Claim 11, characterized by the area of said third semiconductor region facing said gate electrode increasing as the distance from the vicinity of the connecting portion between said gate electrode and said bus line increases.

[Claim 13] A manufacturing method of an insulated gate semiconductor device, characterized by providing
a second semiconductor region formation step for forming a second semiconductor region of a second conductive type in a stripe on a surface region of a first semiconductor region of a first conductive type,

a conductor layer formation step for forming a conductor layer on said first semiconductor region and said second semiconductor region,
a patterning step for forming a striped gate electrode by patterning said conductor layer to form a striped hole exposing an inner surface portion of said second semiconductor region,
a resist pattern formation step for forming a resist pattern intermittently leaving portions of said striped hole,
and a third semiconductor region formation step for injecting and diffusing an impurity of the first conductive type inside said hole using said conductor layer and said resist pattern as a mask to form a third semiconductor region of the first conductive type intermittently exposed on the inside of said striped second semiconductor region.

[Claim 14] The manufacturing method of an insulated gate semiconductor device according to Claim 13, characterized by providing a step for forming a bus line connected to one terminal of said gate electrode and to an external electrode,
and forming said resist pattern in said resist pattern formation step so as to intermittently leave portions of said hole starting from the vicinity of the connecting portion between said gate electrode and said bus line.

[Claim 15] The manufacturing method of an insulated gate semiconductor device according to Claim 14, characterized by forming said resist pattern in said resist pattern formation step such that

said striped second semiconductor region is exposed at a constant width, and the length in the direction in which said exposed portion extends increases as the distance from the vicinity of the connecting portion between said gate electrode and said bus line increases.

[Claim 16] The manufacturing method of an insulated gate semiconductor device according to Claim 14, characterized by forming said resist pattern in said resist pattern formation step such that the area of the second semiconductor region inside said hole increases as the distance from the vicinity of the connecting portion between said gate electrode and said bus line increases.

[Claim 17] The manufacturing method of an insulated gate semiconductor device according to Claim 14, characterized by forming said resist pattern in said resist pattern formation step such that said striped second semiconductor region is exposed at a constant width, and the gap between exposed portions decreases as the distance from the vicinity of the connecting portion between said gate electrode and said bus line increases.

[Claim 18] The manufacturing method of an insulated gate semiconductor device according to Claim 14, characterized by forming said resist pattern in said resist pattern formation step such that the proportion per a specific area occupied by the area of the second semiconductor region exposed inside said hole increases as the distance from the vicinity of the connecting portion between said gate electrode and said bus line increases.

[DETAILED EXPLANATION OF THE INVENTION]

[0001] [INDUSTRIAL FIELD OF APPLICATION]

The present invention relates to an insulated gate semiconductor device with an insulated gate configuration, and a manufacturing method thereof.

[0002] [PRIOR ART]

An IGBT (insulated gate bipolar transistor), which is a type of insulated gate semiconductor device, has low on-resistance and excellent characteristics such as temperature characteristics compared to other types of insulated gate semiconductor devices, and is used, for example, in inverter circuits and power source circuits. A number of techniques for improving these characteristics have been employed in IGBT (see, for example, Patent Literature 1).

[0003] PATENT LITERATURE 1

Japan Kokai Patent Publication 2002-190594

[0004] Fig. 14(a) shows the sectional configuration of a conventional IGBT. As shown in Fig. 14(a), an IGBT has a semiconductor substrate 50 with an n-type base region 51 of relatively low impurity concentration, a p-type collector region 52 of relatively high impurity concentration disposed on the n-face of the n-type base region 51, a p-type base region 53 formed on a surface region of the other face of the n-type base region 51, and an n-type emitter region 54 of relatively high impurity concentration formed on a surface region of the p-type base region 53 of relatively

low impurity concentration.

[0005] A gate electrode 61 disposed on the p-type base region 53 with an insulating film (gate insulating film) 65 in between, and an emitter electrode 62 electrically connected to both the emitter region 54 and the base region 53 are disposed on one face of the semiconductor substrate 50, and a collector electrode 63 connected to the collector region 52 is disposed on the other face. The emitter electrode 62 and the gate electrode 61 are insulated by an interlayer insulating film 64.

[0006] Fig. 14(b) shows a plan view of the IGBT shown in Fig. 14(a), viewed from one face of the semiconductor substrate 50. For easier understanding, Fig. 14(b) omits the emitter electrode 62 and the interlayer insulating film 64.

[0007] As shown in Fig. 14(b), a bus line (gate bus line) 71 is disposed on one face of the semiconductor substrate 50. The bus line 71 has an encircling section 74 disposed near the perimeter of the semiconductor substrate 50, and trunk sections 72 and 73 extending linearly from the encircling section 74 toward the inside. The encircling section 74 has a pad section 75, and is connected by the pad section 75 to an external electrode.

[0008] A plurality of gate electrodes 61 are disposed in comb-teeth stripes from the trunk sections 72 and 73 to both sides. The trunk sections 72 and 73 of the bus line 71 are electrically connected to the gate electrodes 61. That is, the voltage required to

turn the IGBT on is supplied from outside through the bus line 71 to the gate electrodes 61.

[0009] Applying a gate voltage other than the threshold voltage to a gate electrode 61 forms a channel in the p-type base region 53 of the gate electrode 61, making the emitter region 54 and the n-type base region 51 conducting (turning the IGBT on).

[0010] Depending on influences such as the low pass filter formed by the electrical resistance of the gate electrode 61, and the parasitic capacitance between the gate electrode 61 and the channel, this gate voltage is transmitted from the base portion of the gate electrode 61 (the portion near the bus line 71) toward the edge (the tip portion) in the extension direction.

[0011] Thus, applying a gate voltage forms the channel of the IGBT successively from the base portion of the gate electrode 61 toward the tip of this electrode. Therefore, when first applying a gate voltage, the current concentrates, although only for a very short time, in the device region near the trunk sections 72 and 73 of the bus line 71.

[0012] [PROBLEMS THAT THE INVENTION IS TO SOLVE]

If for some reason a load has shorted while the IGBT is turned on and the IGBT is charged with an excessive current, this will result in failure of the IGBT device. The time from when a charging current starts charging the channel until the IGBT fails if the load of an IGBT has shorted under specific conditions is called the load

short-circuit tolerance, and is one of the criteria indicating the performance of an IGBT. That is, the greater this load short-circuit tolerance, the greater the freedom of circuit design and ease of use of the IGBT.

[0013] From the standpoint of this load short-circuit tolerance, an IGBT configured as discussed earlier has had the problem of being prone to latch-up in the portion near the trunk sections 72 and 73, which tends to cause device failure (that is, a low load short-circuit tolerance), due to the time during which a current (electron current) concentrates in the channel formed in the portion near the trunk sections 72 and 73 of the bus line 71 as discussed earlier.

[0014] Such a problem occurs not just in IGBT, but also, for example, in a MISFET (metal insulator semiconductor field effect transistor) with the same configuration as shown in Figs. 14(a) and (b), and other insulated gate semiconductor devices.

[0015] Reflecting on this situation, the object of the present invention is to provide an insulated gate semiconductor device with a large load short-circuit tolerance not prone to latch-up, and a manufacturing method thereof.

[0016] [MEANS OF SOLVING THE PROBLEMS]

To achieve this object, an insulated gate semiconductor device according to a first aspect of the present invention is characterized by providing

a first semiconductor region of a first conductive type,

a second semiconductor region of a second conductive type formed in a stripe on a surface region of the first semiconductor region,

a third semiconductor region of the first conductive type formed on a surface region of the second semiconductor region, and

a striped gate electrode disposed facing the second semiconductor region between the first semiconductor region and the third semiconductor region,

and disposing the third semiconductor region intermittently along the second semiconductor region.

[0017] In this configuration, a bus line connected to one terminal of the gate electrode and to an external electrode may be provided,

and the third semiconductor region may be disposed intermittently along the second semiconductor region starting from the vicinity of the connecting portion between the gate electrode and the bus line.

[0018] In this configuration, the third semiconductor region may be of constant width and disposed such that the length in the direction in which the second semiconductor region extends in a stripe increases as the distance from the vicinity of the connecting portion between the gate electrode and the bus line increases.

[0019] In this configuration, the third semiconductor region may be disposed such that the area facing the gate electrode increases as the distance from the vicinity of the connecting portion between the

gate electrode and the bus line increases.

[0020] In this configuration, the third semiconductor region may be disposed such that its exposed area increases as the distance from the vicinity of the connecting portion between the gate electrode and the bus line increases.

[0021] In this configuration, the third semiconductor region may be of constant width and is disposed such that the gap between the third semiconductor regions decreases as the distance from the vicinity of the connecting portion between the gate electrode and the bus line increases.

[0022] In this configuration, the third semiconductor region may be disposed such that the proportion per a specific area occupied by the exposed area of the third semiconductor region lying within the surface of the second semiconductor region increases as the distance from the vicinity of the connecting portion between the gate electrode and the bus line increases.

[0023] To achieve the object given earlier, an insulated gate semiconductor device according to a second aspect of the present invention is characterized by providing

a first semiconductor region of a first conductive type,

a second semiconductor region of a second conductive type formed in a stripe on a surface region of the first semiconductor region,

a third semiconductor region of the first conductive type formed on a surface region of the second semiconductor region,

a striped gate electrode disposed facing the second semiconductor region between the first semiconductor region and the third semiconductor region, and

a main electrode electrically connected to the second semiconductor region and the third semiconductor region,

and disposing the connecting portion between the second semiconductor region and the main electrode intermittently along the second semiconductor region.

[0024] In this configuration, a bus line connected to one terminal of the gate electrode and to an external electrode may be provided, and the connecting portion may be disposed between the second semiconductor region and the main electrode intermittently along the second semiconductor region starting from the vicinity of the connecting portion between the gate electrode and the bus line.

[0025] In this configuration, the area of the connecting portion between the second semiconductor region and the main electrode may be disposed so as to decrease as the distance from the vicinity of the connecting portion between the gate electrode and the bus line increases.

[0026] In this configuration, the third semiconductor region may be disposed intermittently along the second semiconductor region.

[0027] In this configuration, the area of the third semiconductor region facing the gate electrode may increase as the distance from the vicinity of the connecting portion between the gate

electrode and the bus line increases.

[0028] To achieve the objective given earlier, a manufacturing method of an insulated gate semiconductor device according to a third aspect of the present invention characterized by providing

a second semiconductor region formation step for forming a second semiconductor region of a second conductive type in a stripe on a surface region of a first semiconductor region of a first conductive type,

a conductor layer formation step for forming a conductor layer on the first semiconductor region and the second semiconductor region,

a patterning step for forming a striped gate electrode by patterning the conductor layer to form a striped hole exposing an inner surface portion of the second semiconductor region,

a resist pattern formation step for forming a resist pattern intermittently leaving portions of the striped hole,

and a third semiconductor region formation step for injecting and diffusing an impurity of the first conductive type inside the hole using the conductor layer and the resist pattern as a mask to form a third semiconductor region of the first conductive type intermittently exposed on the inside of the striped second semiconductor region.

[0029] In this method, a step may also be provided for forming a bus line connected to one terminal of the gate electrode and to an

external electrode,

and the resist pattern may be formed in the resist pattern formation step so as to intermittently leave portions of the hole starting from the vicinity of the connecting portion between the gate electrode and the bus line.

[0030] In this method, the resist pattern may be formed in the resist pattern formation step such that the striped second semiconductor region is exposed at a constant width, and the length in the direction in which the exposed portion extends increases as the distance from the vicinity of the connecting portion between the gate electrode and the bus line increases.

[0031] In this method, the resist pattern may be formed in the resist pattern formation step such that the area of the second semiconductor region inside the hole increases as the distance from the vicinity of the connecting portion between the gate electrode and the bus line increases.

[0032] In this method, the resist pattern may be formed in the resist pattern formation step such that the striped second semiconductor region is exposed at a constant width, and the gap between exposed portions decreases as the distance from the vicinity of the connecting portion between the gate electrode and the bus line increases.

[0033] In this method, the resist pattern may be formed in the resist pattern formation step such that the proportion per a specific

area occupied by the area of the second semiconductor region exposed inside the hole increases as the distance from the vicinity of the connecting portion between the gate electrode and the bus line increases.

[0034] [EMBODIMENT OF THE INVENTION]

Next, an insulated gate semiconductor device according to a first embodiment of the present invention will be discussed in detail, referring to the appended drawings, taking the example of an insulated gate bipolar transistor (IGBT).

[0035] Fig. 1(a) shows a plan view of an IGBT of a first embodiment, and Fig. 1(b) shows a partially enlarged view of this IGBT. Figs. 2(a) and 2(b) show section views from line A-A and line B-B of the IGBT.

[0036] To facilitate understanding, Figs. 1(a) and (b) omit the emitter electrode 32 and the interlayer insulating film 34, to be discussed later.

[0037] The IGBT according to the first embodiment has an essentially rectangular semiconductor substrate 10 as shown in Fig. 1(a).

[0038] As shown in Fig. 2(a), the IGBT has the semiconductor substrate 10, a gate electrode 31, an emitter electrode 32, and a collector electrode 33 as shown in the section view from line A-A of Fig. 1(b).

[0039] The semiconductor substrate 10 has an n-type base region

11, a collector region 12, a p-type base region 13, and emitter regions 14.

[0040] The n-type base region 11 comprises an n-type semiconductor region doped with an n-type impurity such as phosphorus (P) or arsenic (As). The n-type base region 11 constitutes one face of the semiconductor substrate 10. The n-type base region 11 comprises, for example, an n-type semiconductor substrate such as a silicon monocrystalline substrate.

[0041] The collector region 12 comprises a semiconductor region doped with a p-type impurity, such as boron (B) or aluminum (Al), at a higher impurity concentration than the p-type base region 13 to be discussed later. The collector region 12 constitutes the other face of the semiconductor substrate 10. The collector region 12 is formed, for example, by introducing a p-type impurity into one face of the n-type semiconductor region comprising the n-type base region 11.

[0042] The p-type base region 13 comprises a p-type semiconductor region doped with a p-type impurity and disposed on a surface region of the n-type base region 11. Although two regions are shown in the drawing, two or more of the p-type base region 13 may be disposed, separated by a specific gap.

[0043] The emitter regions 14 comprise n-type semiconductor regions doped with an n-type impurity at a higher impurity concentration than the n-type base region 11 and disposed on surface regions of the p-type base region 13. Emitter regions 14 are disposed

on the outer edges of the p-type base region 13 in the Y direction. In other words, a plurality of emitter regions 14 are disposed on a surface region of each p-type base region 13 so as to arrange in two rows along the X direction separated by a specific gap. As will be discussed later, the p-type base regions 13 held between a plurality of n-type base regions 11 and emitter regions 14 comprise channel formation regions.

[0044] The gate electrode 31 is disposed so as to cover at least the p-type base region (the channel formation region) held between the n-type base region 11 and the emitter region 14. The gate electrode 31 comprises, for example, a polysilicon film formed by CVD (chemical vapor deposition).

[0045] A gate insulating film 35 comprising, for example, a silicon oxide film is disposed between the gate electrode 31 and the channel formation region. The gate electrode 31 and the gate insulating film 35 comprise the gate of the IGBT.

[0046] The face of the semiconductor substrate 10 containing the face of the gate electrode 31 is covered by an interlayer insulating film 34 comprising, for example, a silicon oxide film. Opening holes 36 have been made in the interlayer insulating film 34 so as to expose the inner side of the p-type base region 13 and the inner sides of two emitter regions 14 inside this base region at the bottom of the holes.

[0047] As shown in the plan view of Fig. 1(a), a plurality of

gate electrodes 31 is disposed on one face of the semiconductor substrate 10 arranged and separated by a specific gap and disposed extending in the X direction.

[0048] A bus line (gate bus line) 20 for connecting the gate electrodes 31 to an external electrode is disposed on one face of the semiconductor substrate 10. The bus line 20 is formed, for example, by laminating a metallic film such as aluminum over a polysilicon film formed by the same step as the gate electrodes 31.

[0049] The bus line 20 forms a stripe of a specific width, and has an encircling section 22 forming a frame along the edges of the semiconductor substrate 10. A striped first trunk section 23 and second trunk section 24 extend, one in the Y direction and the other in the -Y direction, from essentially the center of the two opposite long sides of the encircling section 22.

[0050] The first trunk section 23 and the second ice cube button 24 are extended in opposite directions on the same line. The ends of the two trunk sections are disposed near the center of the semiconductor substrate 10 not in contact with each other and are separated by a specific gap.

[0051] The plurality of gate electrodes 31 is disposed to collectively form comb teeth extending essentially perpendicularly from the two (long) sides of the first and second trunk sections 23 and 24. The length of the gate electrodes 31 in the extension direction is set slightly shorter than the length from the sides of

the first and second trunk sections 23 and 24 to the short sides of the encircling section 22. That is, the gate electrodes 31 have been configured such that one terminal contacts the sides of the first or second trunk section 23 or 24, and the other terminal does not contact the encircling section 22.

[0052] One short side of the encircling section 22 is electrically connected to a bonding pad 21 comprising, for example, aluminum. The bonding pad 21 may be formed together with the bus line 20. A bonding wire (not shown) is connected to the bonding pad 21, and an external voltage is applied through this bonding wire. The applied voltage is applied to the gate electrodes 31 through the first and second trunk sections 23 and 24 of the bus line 20.

[0053] As shown in the expanded view of Fig. 1(b), p-type base regions 13 are formed so as to expose the face of the semiconductor substrate 10 along the gate electrodes 31 extending in the X direction with the first and second trunk sections 23 and 24 as one terminal. The p-type base regions 13 are disposed forming comb teeth in the X direction in the same way as the gate electrodes 31.

[0054] Emitter regions 14 are exposed inside the p-type base regions 13 as discussed earlier. The emitter regions 14 are formed such that essentially rectangular exposed faces are arranged on the same line in the X direction separated by a specific gap. In other words, the emitter regions 14 are disposed inside the exposed faces of the p-type base regions 13 so as to expose intermittent islands.

Therefore, the p-type base regions 13 has regions where no emitter region 14 has been disposed, as shown by the section view from line B-B in Fig. 2(b).

[0055] As shown in Fig. 1(b), the emitter region 14 has an essentially constant width in the Y direction, and has been formed such that the length in the extension direction gradually increases as the distance (facing the X direction) from the connecting portion between the gate electrode 31 and the first trunk section 23 increases.

[0056] The area of the exposed faces of the emitter regions 14 is smaller near the connecting portion between the gate electrode 31 and the first or second trunk section 23 or 24, and the area of the exposed faces of the emitter regions 14 becomes greater farther from this connecting portion.

[0057] The emitter regions 14 are also disposed such that the area facing the gate electrodes 31 gradually increases in the extension direction.

[0058] In Fig. 1(b), emitter regions 14 with substantially the same exposed area have been formed two at a time continuously arranged along the X direction.

[0059] Referring to Fig. 2(a), the emitter electrode 32 is packed inside the opening hole 36, and disposed so as to electrically connect the p-type base region 13 to the emitter region 14. The emitter electrode 32 comprises, for example, an aluminum film formed

by PVD (physical vapor deposition), and is formed as a continuous film buried inside a plurality of opening holes 36.

[0060] The collector electrode 33 comprises, for example, an aluminum film formed, for example, by PVD, and is disposed on the collector region 12 on the other face of the semiconductor substrate 10. Therefore, the collector electrode 33 contacts the collector region 12.

[0061] Next, the manufacturing method of an IGBT configured in this way will be discussed referring to Figs. 3(a) to (d) and Figs. 4(e) to (g). The steps discussed below are one example, and any steps may be used so long as they produce the same configuration.

[0062] First, an n-type semiconductor substrate 10 doped with an n-type impurity is prepared. Next, a p-type impurity is diffused in the lower face of the semiconductor substrate 10 to form a p-type semiconductor layer with a higher impurity concentration than the p-type base region 13 to be formed later as shown in Fig. 3(a). This forms the collector region 12 discussed earlier.

A p-type epitaxial layer may also be formed on the n-type substrate.

[0063] Next, an oxide treatment, for example, is applied to the upper face of the semiconductor substrate 10 to form a silicon oxide film 40 as shown in Fig. 3(b). A polysilicon film is then formed on the silicon oxide film 40, for example, by CVD. Following this, the polysilicon film and the silicon oxide film 40 are patterned using,

for example, photolithography to form an opening hole 37 as shown in Fig. 3(c). This forms gate electrodes 31 and gate insulating films 35 in a comb-teeth shape.

[0064] Next using the polysilicon film forming the gate electrodes 31 as a mask, a p-type impurity is injected in the n-type base region 11, for example, by ion injection to form a p-type semiconductor region, namely, the p-type base region 13 as shown in Fig. 3(d).

[0065] Next, a resist is applied to the front of the semiconductor substrate 10 and developed by exposing to form a resist pattern 42 as shown in Fig. 4(e). The resist pattern 42 is disposed so as to intermittently leave striped portions of the opening holes 37 in the polysilicon film as shown in Fig. 5.

[0066] The resist pattern 42 is disposed on “skipped” regions where an emitter region 14 will not be formed in the p-type base region 13. As shown in Fig. 5, the resist pattern 42 has narrow portions 42a with a narrow width in the Y direction, and wide portions 42b with a wide width in the Y direction. The length of each wide portion 42b in the X direction in Fig. 5 is determined by the gap in the X direction between emitter regions 14, and the gap between wide portions 42b is determined by the length (and by extension, the exposed area) of the emitter regions 14 in the X direction.

[0067] For example, forming the resist pattern 42 such that the

length of the p-type base region 13 exposed in the opening hole 37 increases farther (facing the X direction) from the connecting portion between the first or second trunk section 23 or 24 and the gate electrodes 31 can form emitter regions 14 which gradually increase in length and exposed area in the extension direction as shown in Fig. 1(b).

[0068] Using the polysilicon film formed with such a resist pattern 42 as a mask, an n-type impurity is injected in the p-type base region 13, for example, by ion injection. At the same time, an impurity is introduced into the polysilicon film to give a desired conductivity. After introducing an impurity, the resist pattern 42 is removed by ashing.

[0069] Introducing an impurity prevents introducing an impurity into the emitter skipped regions while forming n-type semiconductor regions in the emitter formation regions. Next, the n-type semiconductor regions are diffused to form emitter regions 14 as shown in Fig. 4(f). This forms emitter regions 14 arranged intermittently as shown in Fig. 1(b).

[0070] Next, a silicon oxide film is formed on the upper face of the semiconductor substrate 10, for example, by CVD so as to cover the gate electrodes 31. A heat treatment then stabilizes the quality of the silicon oxide film and flattens its surface. Next, the silicon oxide film is etched to form an interlayer insulating film 34 with opening holes 36 as shown in Fig. 4(g).

[0071] Next, a metallic film, such as an aluminum film, is formed on the upper face of the semiconductor substrate 10, for example, by PVD. Patterning this film forms an emitter electrode 32 electrically connected to the p-type base region 13 and the emitter region 14 through the opening hole 36. This patterning also forms a bus line 20 and a bonding pad 21 as shown in Fig. 1(a).

[0072] Next, a collector electrode 33 comprising, for example, an aluminum film is formed on the lower face of the semiconductor substrate 10, for example, by PVD. These steps form an IGBT with the planar shape shown in Fig. 1(a) and a cross section such as shown in Figs. 2(a) and 2(b).

[0073] Next, the operation of the IGBT of the first embodiment with this configuration will be discussed.

First, applying a voltage to the gate electrodes 31 of the IGBT through the first and second trunk sections 23 and 24 of the bus line 20 generates an electric field, which forms a depletion layer in a surface region of the p-type base region 13 below the gate insulating film 35. Increasing the applied voltage above a threshold voltage forms an inversion layer (n-channel) in the surface region of the p-type base region 13.

[0074] As a result, electrons are injected from the emitter regions 14 through the channel into the n-type base region 11, and positive holes are injected from the collector region 12 into the n-type base region 11. Therefore, a current charges between the emitter

regions 14 and the collector region 12 through the channel and the n-type base region 11, turning the IGBT on. This current also charges from the emitter electrode 32 through the p-type base region 13 to outside.

[0075] The gate voltage applied to the gate electrodes 31 is transmitted from the bus line 20 toward the tips of the gate electrodes 31 with a delay due to the influence of a low pass filter, for example, formed by the parasitic voltage between the gate electrodes 31 and the channel. Therefore, when the gate voltage is first applied, a relatively large current concentrates, although only for a very short time, in the device region near the connecting portion between the first and second trunk sections 23 and 24 of the bus line 20.

[0076] If for any reason a load has shorted during this time and the IGBT is charged with an excessive current, a so-called latch-up tends to occur, especially in the device region near the connecting portion between the first and second trunk sections 23 and 24 of the bus line 20.

[0077] This latch-up will be discussed referring to Fig. 6. "Latch-up" refers to a phenomenon in which an increase in the (positive-hole) current from the other side of the substrate causes a potential difference due to the resistance (R_B) just below the emitters on the route of this positive-hole current, and the resulting potential difference turns on a parasitic thyristor based

on the gate voltage. When latched up, the current charging from the collector to the emitter of the IGBT charges the parasitic thyristor, making it impossible to control the gate voltage of the IGBT. As a result, the latched-up IGBT suffers a device failure.

[0078] In the IGBT of the first embodiment, emitter regions 14 have been arranged intermittently exposed along the direction in which the p-type base region 13 extends, and formed such that their length in the extension direction increases as the distance from the connecting portion with the first or second trunk section 23 or 24 increases. As a result, the area of the connecting portion between the p-type base region 13 and the emitter electrode 32 widens near the connecting portion between the first or second trunk section 23 or 24 and the gate electrodes 31 and narrows farther from this connecting portion.

[0079] As discussed earlier, the gate electrodes 31 and the region near the connecting portion with the first and second trunk sections 23 and 24 of the bus line 20 are the first regions in the device to turn on. The length of the emitter regions 14 in the extension direction, however, is short near the first and second trunk sections 23 and 24. Therefore, the electron current charging from the emitter regions 14 to the p-type base region 13 is limited to a relatively small current by the relatively small exposed area, and by extension, the area facing the gate electrodes 31. As a result, the positive-hole current charged from the collector is

relatively small in the emitter regions 14 near the first and second trunk sections 23 and 24, and thus satisfactorily prevents latch-up.

[0080] Thus, the IGBT of the first embodiment has a large margin against latch-up near the first and second trunk sections 23 and 24 of the bus line 20, satisfactorily prevents a parasitic thyristor latching up due to a concentration of current if first turned on while a load has shorted, and has high failure resistance.

[0081] Next, an insulated gate semiconductor device according to a second embodiment of the present invention will be discussed referring to the drawings, taking the example of an insulated gate bipolar transistor (IGBT).

[0082] The IGBT of the second embodiment differs from the first embodiment in the formation region of the emitter regions 14. The rest of the configuration is essentially the same as the first embodiment.

[0083] Fig. 7 shows a partially expanded view of the IGBT according to the second embodiment. To facilitate understanding, Fig. 7 omits the emitter electrode 32 and the interlayer insulating film 34.

[0084] In the second embodiment, the emitter region 14 comprises an n-type semiconductor region doped with an n-type impurity at a higher impurity concentration than the n-type base region 11 and disposed on a surface region of the p-type base region 13 in the same way as the first embodiment

[0085] In the second embodiment, however, as shown in Fig. 7, the emitter regions 14 are formed with an essentially constant length in the X direction and length in the Y direction, and the gap between these emitter regions in the extension direction gradually narrows as the distance (facing the X direction) from the connecting portion between the gate electrodes 31 and the first trunk section 23 increases.

[0086] As a result, the proportion of the exposed area on the surface of the p-type base region 13 occupied by the emitter regions 14 per a given constant specific area drops moving closer the connecting portion between the gate electrodes 31 and the first or second trunk section 23 or 24, and gradually increases moving away from the connecting portion with the first trunk section 23.

The rest of the configuration is essentially the same as the configuration shown for the first embodiment.

[0087] The gap between emitter regions 14 may ultimately become zero to form a plurality of continuous emitter regions 14.

[0088] Next, the manufacturing method of an IGBT according to the second embodiment will be discussed. The steps discussed below are one example, and any steps may be used so long as they produce the same configuration.

[0089] Preparation of an n-type semiconductor substrate 10 doped with an n-type impurity through formation of a p-type base region 13 are essentially the same as the first embodiment (Figs. 3(a) to

3(d)).

[0090] After forming the p-type base region 13, a resist is applied to the front of the semiconductor substrate 10 and developed by exposing to form a resist pattern 45 as shown in Fig. 8(a). The resist pattern 45 is disposed so as to intermittently leave striped portions of the opening holes 37 in the polysilicon film as shown in Fig. 8(b).

[0091] The resist pattern 45 has narrow portions 45a with a narrow width in the Y direction and wide portions 45b with a wide width in the Y direction, and is disposed on “skipped” regions where an emitter region 14 will not be formed in the p-type base region 13 as in the first embodiment.

[0092] In the second embodiment, however, the gaps between wide portions 45b are essentially equal, as shown in Fig. 8(b). The wide portions 45b are also formed such that the length in the X direction becomes shorter as the distance (facing the X direction) between the first or second trunk section 23 or 24 and the gate electrodes 31 increases.

This procedure can form emitter regions 14 with gradually narrowing gaps in the extension direction as shown in Fig. 7.

[0093] Using the polysilicon film formed with such a resist pattern 45 as a mask, an n-type impurity is injected into the p-type base region 13, for example, by ion injection. At the same time, an impurity is introduced into the polysilicon film to give a desired

conductivity. After introducing an impurity, the resist pattern 45 is removed by ashing.

[0094] Introducing an impurity prevents introducing an impurity into the emitter skipped regions while forming n-type semiconductor regions in the emitter formation regions. Next, the n-type semiconductor regions are diffused to form emitter regions 14 arranged intermittently as shown in Fig. 7.

[0095] Thereafter, essentially the same steps as the first embodiment are carried out to form an IGBT with emitter regions 14 as shown in Fig. 7.

[0096] As indicated in the first embodiment, the gate electrodes 31 and the region near the connecting portion with the first and second trunk sections 23 and 24 of the bus line 20 are the first regions in the device to turn on. In the second embodiment, however, the gap between emitter regions 14 is wide in the region near the first and second trunk sections 23 and 24, and the gap between emitter regions 14 narrows farther from the first and second trunk sections 23 and 24.

[0097] Varying the gap between emitter regions 14 in the second embodiment in this way increases the size of the holes for drawing positive holes (the area of the connecting portion between the p-type base region 13 and the emitter electrode 32) near the connecting portion between the first or second trunk section 23 or 24 and the gate electrodes 31, and decreases this size moving away from the

connecting portion. This results in increased resistance to the positive-hole current near the connecting portion, and satisfactorily prevents a parasitic thyristor latching up due to a concentration of current if first turned on while a load has shorted. That is, the IGBT according to the second embodiment has high failure resistance.

[0098] The present invention is not limited to these first and second embodiments, and permits numerous variants and applications.

For example, the IGBT indicated in these first and second embodiments may be configured with the reverse polarities.

[0099] In the first embodiment discussed earlier, emitter regions 14 with the same exposed area were arranged two at a time continuously in the X direction. The emitter regions are not limited to this configuration, however, and can be configured non-continuously with the same exposed area, or continuously with three or more exposed areas.

[0100] Although the first and second embodiments discussed earlier showed formation of emitter regions 14 arranged in two rows in the X direction within the same p-type base region 13, the emitter regions 14 may also be formed arranged in one row in the same p-type base region 13. If possible, emitter regions 14 may also be formed arranged in three or more rows within the same p-type base region 13.

[0101] For example, the first embodiment may be configured by disposing emitter regions 14 in just one row in the X direction on each p-type base region 13 as shown in Fig. 9. In this case, the

resist pattern 42 discussed earlier is formed as shown in Figs. 10(a) and (b).

[0102] That is, the resist pattern 42 comprises just wide portions 42b with no narrow portions 42a. Specifically, each resist pattern 42 (each wide portion 42b) is substantially equal in length in the X direction, and the gap between resist patterns 42 increases farther (facing the X direction) from the connecting portion between the first or second trunk section 23 or 24 and the gate electrodes 31.

[0103] Injecting an n-type impurity into the p-type base region 13 using such a resist pattern 42 as a mask can form emitter regions 14 as shown in Fig. 9.

[0104] The second embodiment may also be configured, for example, by disposing emitter regions 14 in just one row along the X direction on each p-type base region 13 as shown in Fig. 11. In this case, the resist pattern 45 discussed earlier is formed as shown in Figs. 12(a) and (b).

[0105] That is, the resist pattern 45 comprises just wide portions 45b with no narrow portions 45a. Specifically, the gaps between resist patterns 45 (wide portions 45b) in the X direction are substantially equal, and the length of each resist pattern 45 in the X direction decreases farther (facing the X direction) from the connecting portion between the first or second trunk section 23 or 24 and the gate electrodes 31.

[0106] Injecting an n-type impurity into the p-type base region 13 using such a resist pattern 45 as a mask can form emitter regions 14 as shown in Fig. 11.

[0107] Although the shape of the portions where emitter regions 14 have not been formed (the holes for drawing positive holes) is shown as square in Figs. 9 and 11, so long as the p-type base region 13 can be exposed on the front of the n-type base region 11, this shape can be any shape, such as circular or elliptical.

[0108] Varying the gap between emitter regions 14 and the exposed area of the emitter regions 14 on the front of the semiconductor substrate 10, as discussed earlier, can facilitate decreasing the size of the holes for drawing positive holes moving away from the connecting portion between the first or second trunk section 23 or 24 and the gate electrodes 31. So long as the size of the holes for drawing positive holes can decrease moving away from this connecting portion, however, the gap between emitter regions 14 and the exposed area of the emitter regions 14 may be constant. For example, an insulating film with a pattern designed to decrease the size of the holes for drawing positive holes moving away from this connecting portion may be formed on the semiconductor substrate 10, and the emitter electrode 32 formed on this insulating film.

[0109] The embodiments of the present invention were discussed taking the example of an IGBT, but are not limited to this example. The present invention obtains comparable effects applied, for

example, to metal insulator semiconductor field effect transistors (MISFET) and other insulated gate semiconductor devices.

[0110] In this case, for example, the collector region 12 of the IGBT discussed earlier may be omitted, the emitter region 14 may be a source region, and the n-type base region 11 may be a drain region.

[0111] The first and second embodiments discussed examples in which the gate electrodes 31 had one terminal connected to the first or second trunk section 23 or 24 of the bus line 20, and the other terminal connected to the encircling section 22 of the bus line 20. As shown in Fig. 13, however, the length of the gate electrodes 31 may equal the distance from the long sides of the first and second trunk sections 23 and 24 to the short sides of the encircling section 22, to configure the gate electrodes 31 to connect with both of these sections.

[0112] In this case, the exposed area of the emitter regions 14 may gradually increase from the vicinity of the encircling section 22 and the first or second trunk section 23 or 24 toward the center of the gate electrodes 31. Alternately, the gap between emitter regions 14 may narrow from the vicinity of the encircling section 22 and the first or second trunk section 23 or 24 toward the center of the gate electrodes 31. Such a configuration satisfactorily prevents latch-up in the vicinity of the connecting portion between the bus line 20 and both terminals of the gate electrodes 31.

[0113] [EFFECTS OF THE INVENTION]

As discussed above, the present invention provides an insulated gate semiconductor device with a large load short-circuit tolerance not prone to latch-up, and a manufacturing method thereof.

[BRIEF EXPLANATION OF THE DRAWINGS]

FIG. 1: Fig. 1(a) is a plan view of an IGBT according to a first embodiment, and Fig. 1(b) is a partially expanded view of the IGBT in Fig. 1(a).

FIG. 2: Fig. 2(a) is a section view from line A-A of the IGBT shown in Fig. 1(b), and Fig. 2(b) is a section view from line B-B of the IGBT shown in Fig. 1(b).

FIG. 3: Figs. 3(a) to 3(d) are diagrams showing the manufacturing process of an IGBT.

FIG. 4 Figs. 4(e) to 4(g) are diagrams showing the manufacturing process of an IGBT.

FIG. 5 is a diagram showing the formation method of an emitter skipped region.

FIG. 6 is a diagram illustrating latch-up.

FIG. 7 is a partially expanded view of an IGBT according to a second embodiment.

FIG. 8 is a diagram showing the formation method of an emitter skipped region for realizing the configuration shown in Fig. 7.

FIG. 9 is a diagram showing a variant of the present invention.

FIG. 10 is a diagram showing the formation method of an emitter

skipped region for realizing the configuration shown in Fig. 9.

FIG. 11 is a diagram showing a variant of the present invention.

FIG. 12 is a diagram showing the formation method of an emitter skipped region for realizing the configuration shown in Fig. 11.

FIG. 13 is a diagram showing a variant of the present invention.

FIG. 14: Fig. 14(a) is a section view of a conventional IGBT, and Fig. 14(b) is a plan view.

[EXPLANATION OF THE REFERENCE NUMERALS]

10 Semiconductor substrate

11 n-Type base region

12 Collector region

13 p-Type base region

20 Bus line

21 Bonding pad

22 Encircling section

23, 24 First and second trunk sections

31 Gate electrode

32 Emitter electrode

33 Collector electrode

34 Interlayer insulating film

42 Resist pattern

45 Resist pattern

FIG. 1

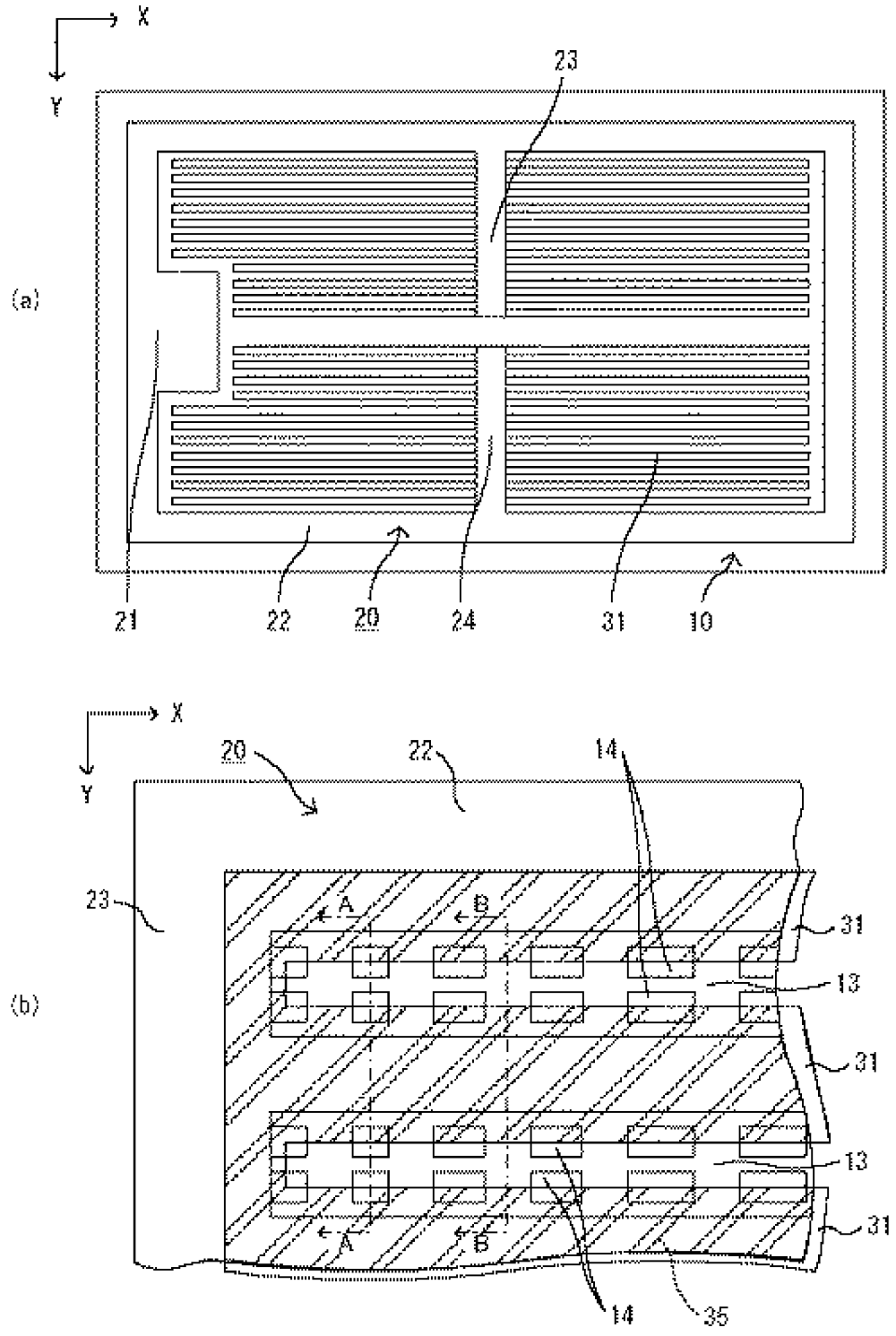
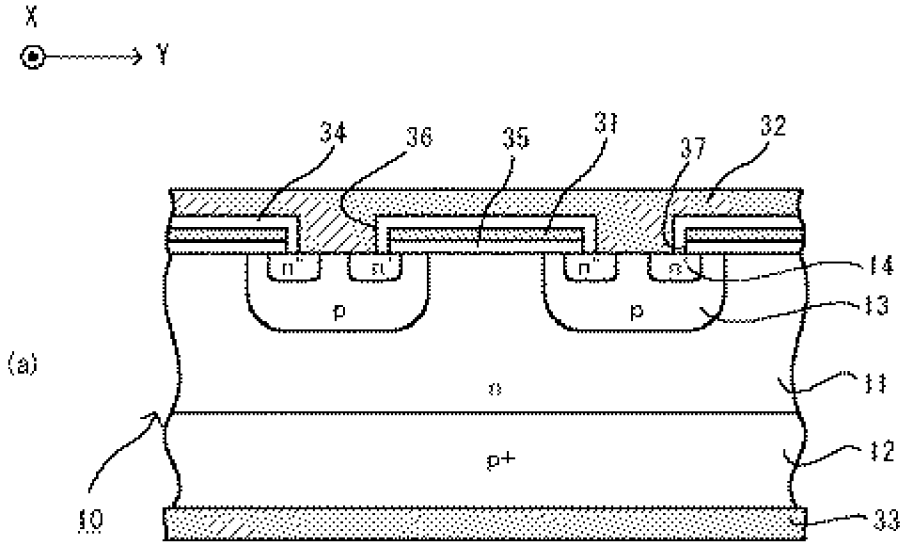
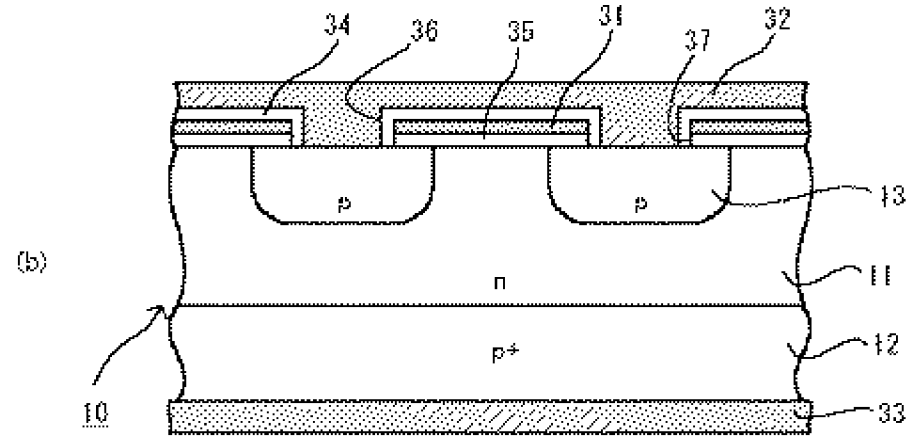


FIG. 2


X
Y
(a)
34
36
35
31
37
32
n+
n+
n+
n+
p
p
14
13
n
11
p+
12
10
33

A—A


(b)
34
36
35
31
37
32
p
p
13
n
11
p+
12
10
33

B—B

FIG. 3

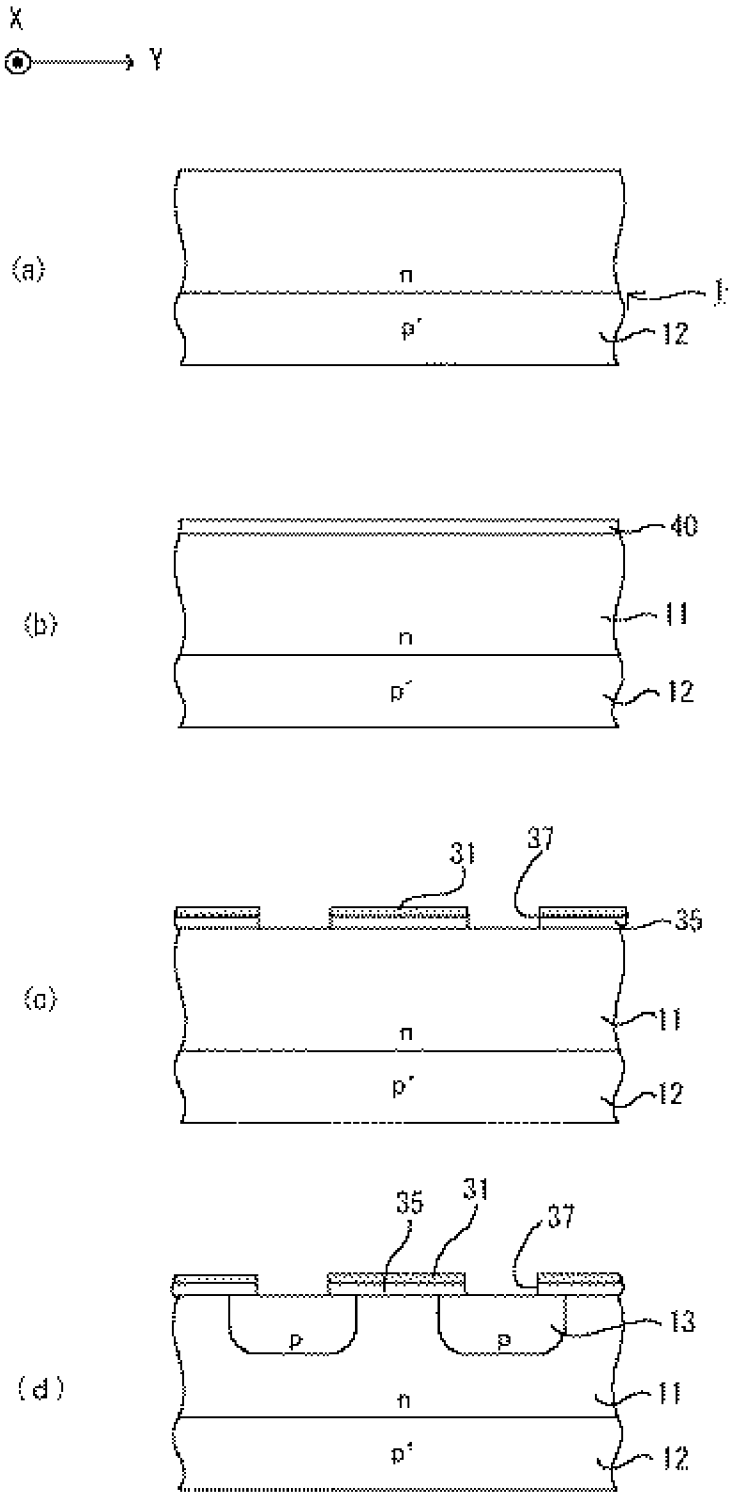


FIG. 4

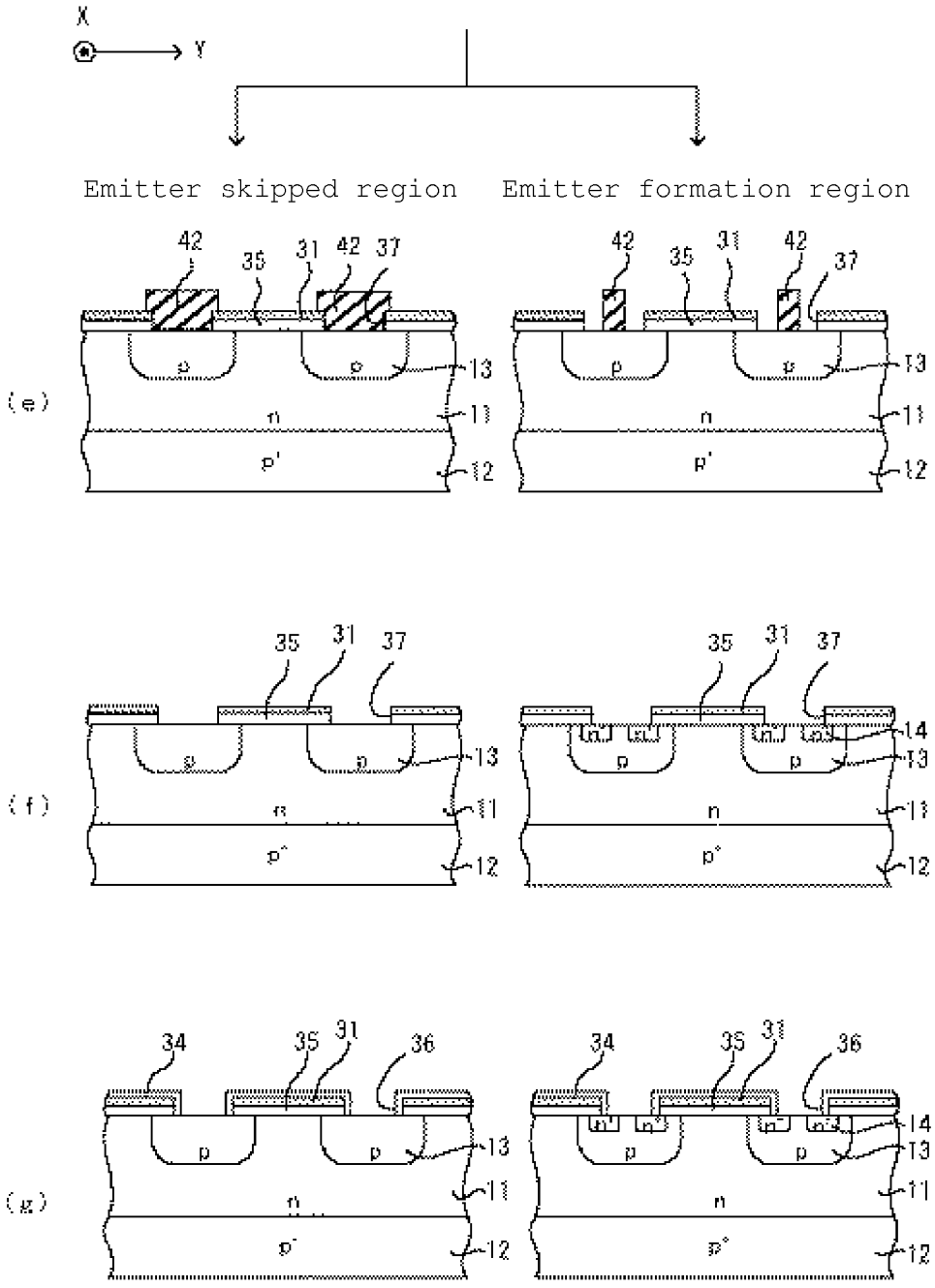

X
Y
Emitter skipped region
Emitter formation region
(e)
(f)
(g)
42
35
31
37
34
36
p
n
p+
p-
11
12
13
14

FIG. 5

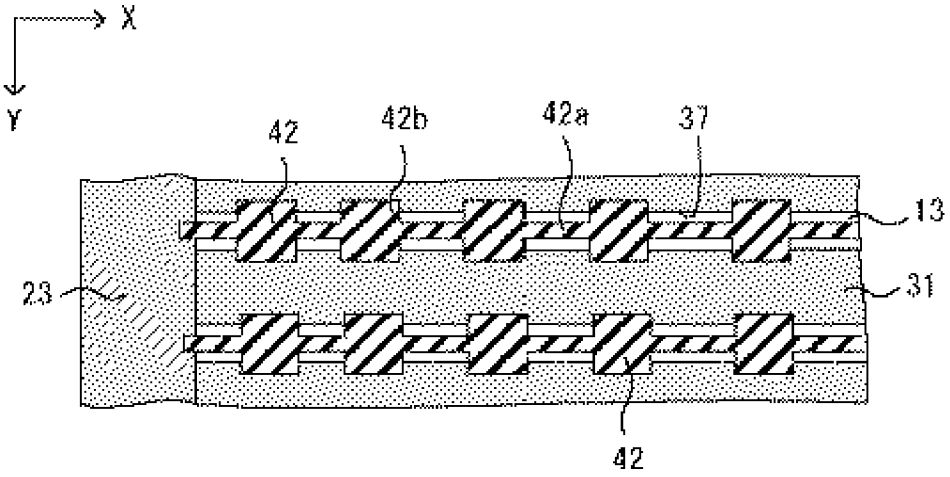


FIG. 6

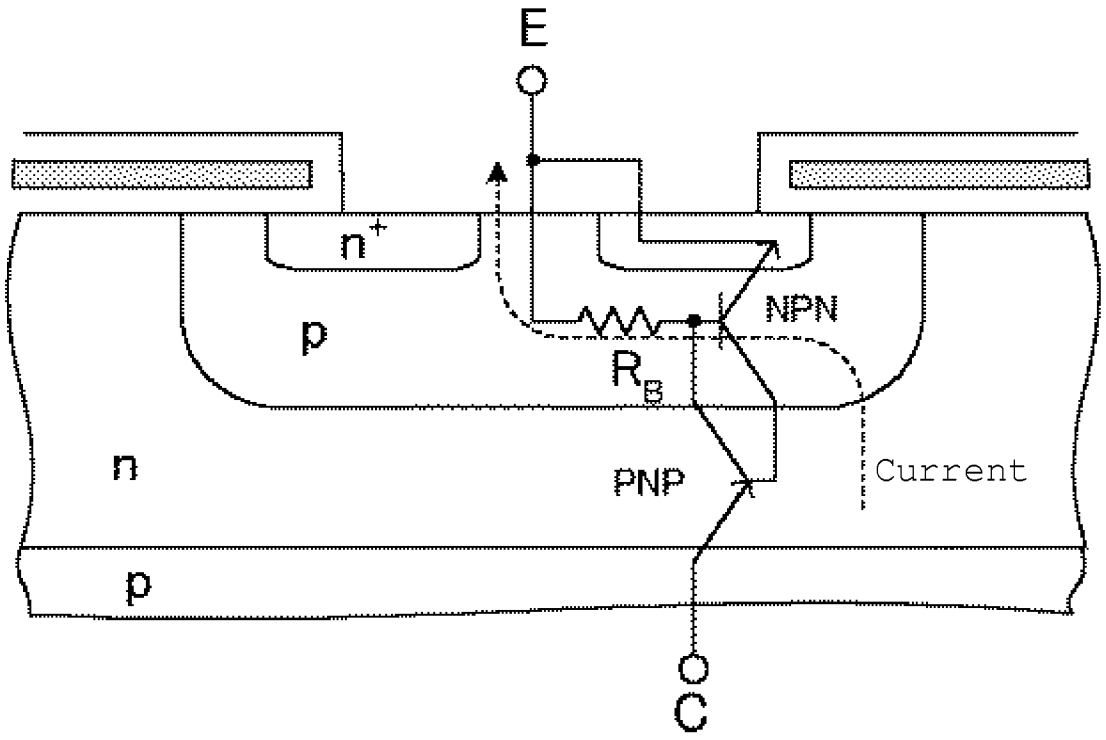


FIG. 7

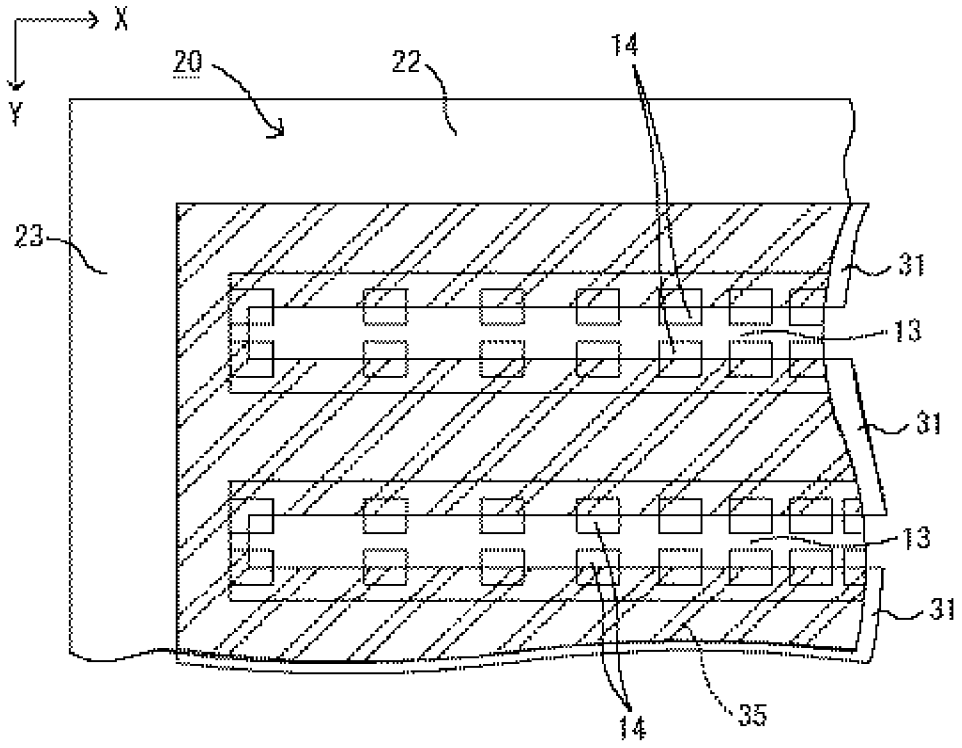


FIG. 8

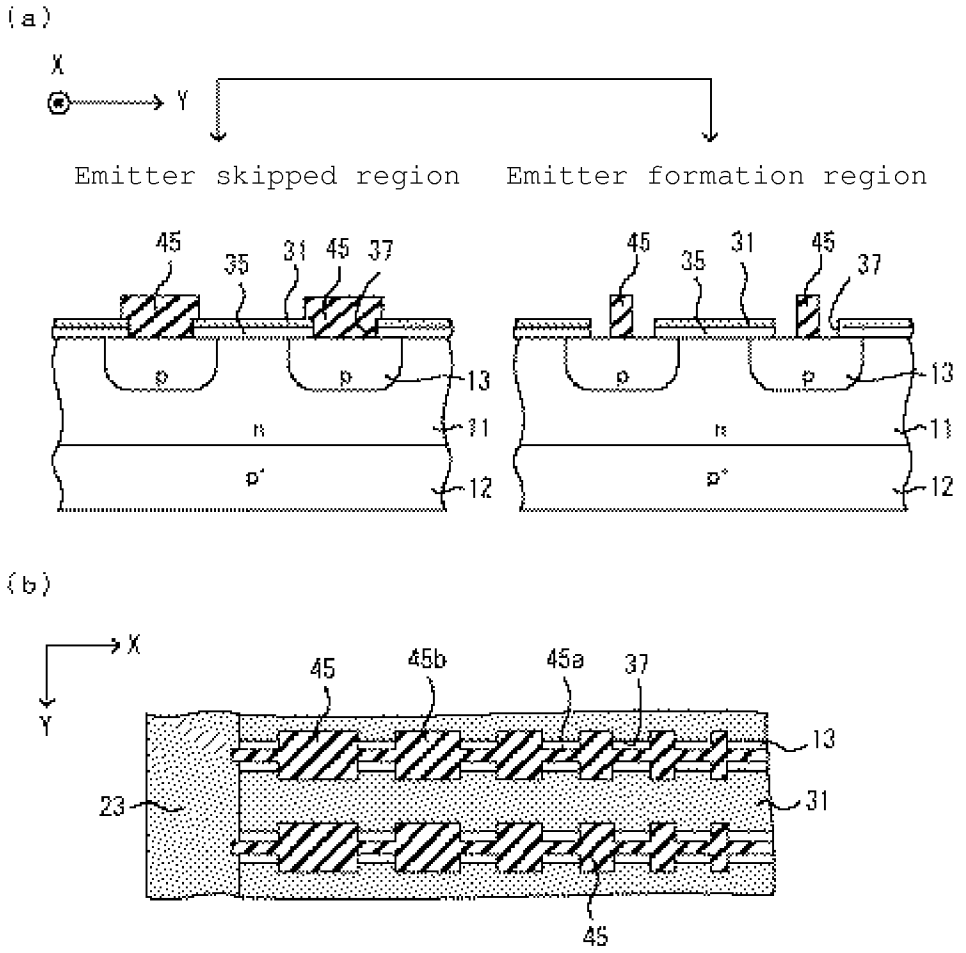

(a)
X
Y
Emitter skipped region
Emitter formation region
45
35
31
45
37
p
p
13
n
11
p+
12
(b)
X
Y
45
45b
45a
37
13
23
31
45

FIG. 9

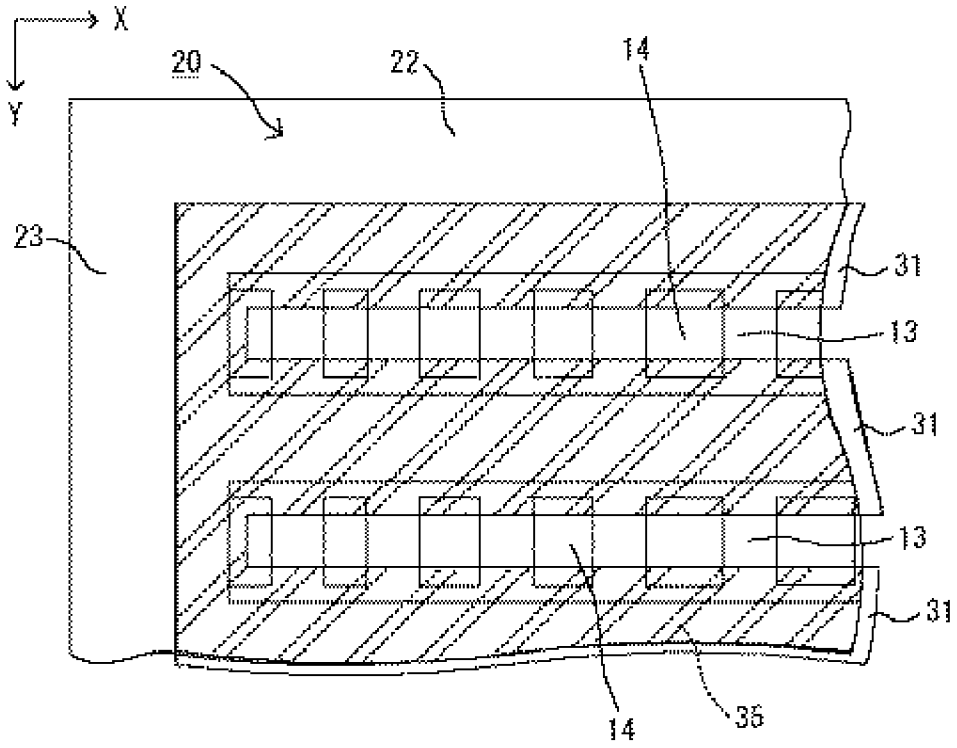


FIG. 10

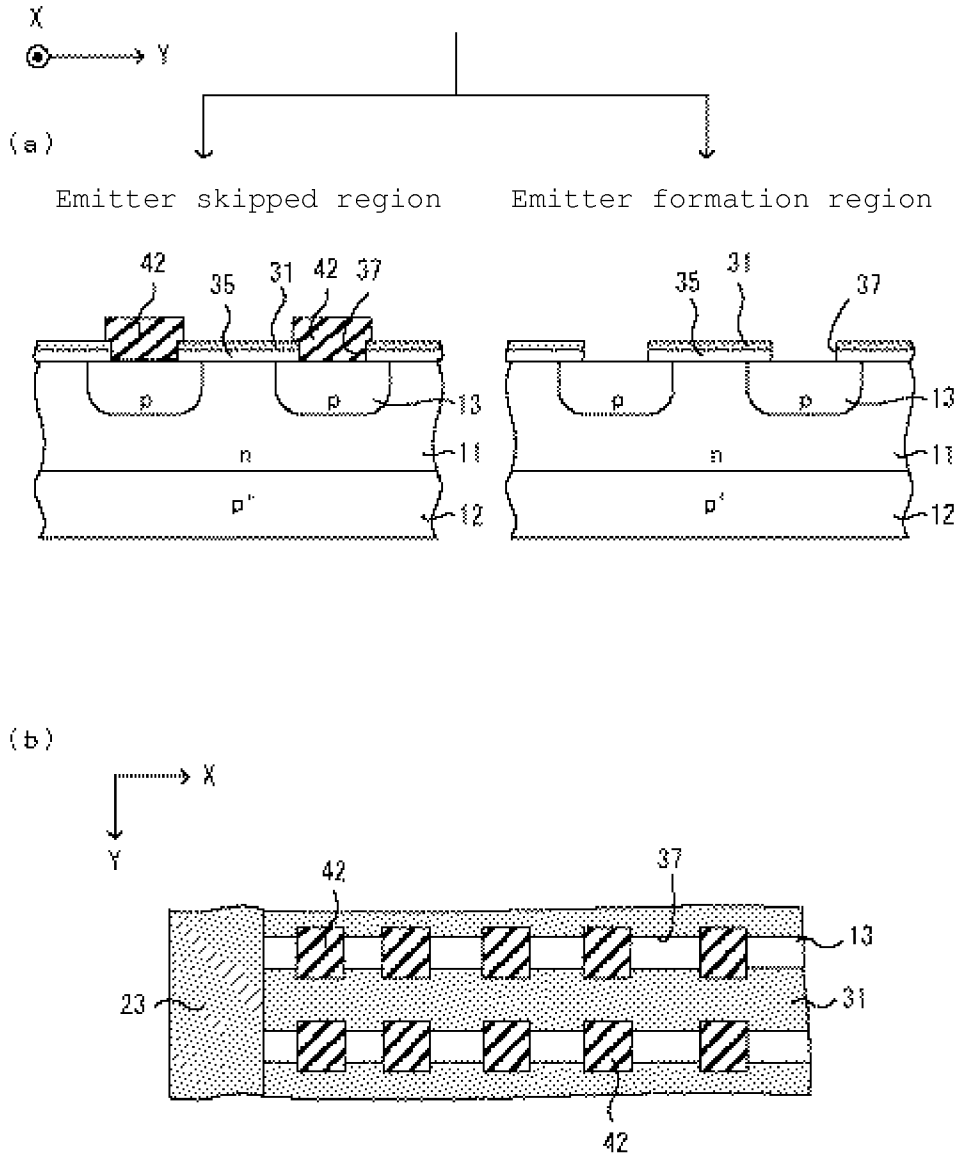

X
Y
(a)
Emitter skipped region
Emitter formation region
42
35
31
42
37
p
p
13
n
11
p+
12
35
31
37
p
p
13
n
11
p+
12
(b)
X
Y
42
37
13
23
31
42

FIG. 11

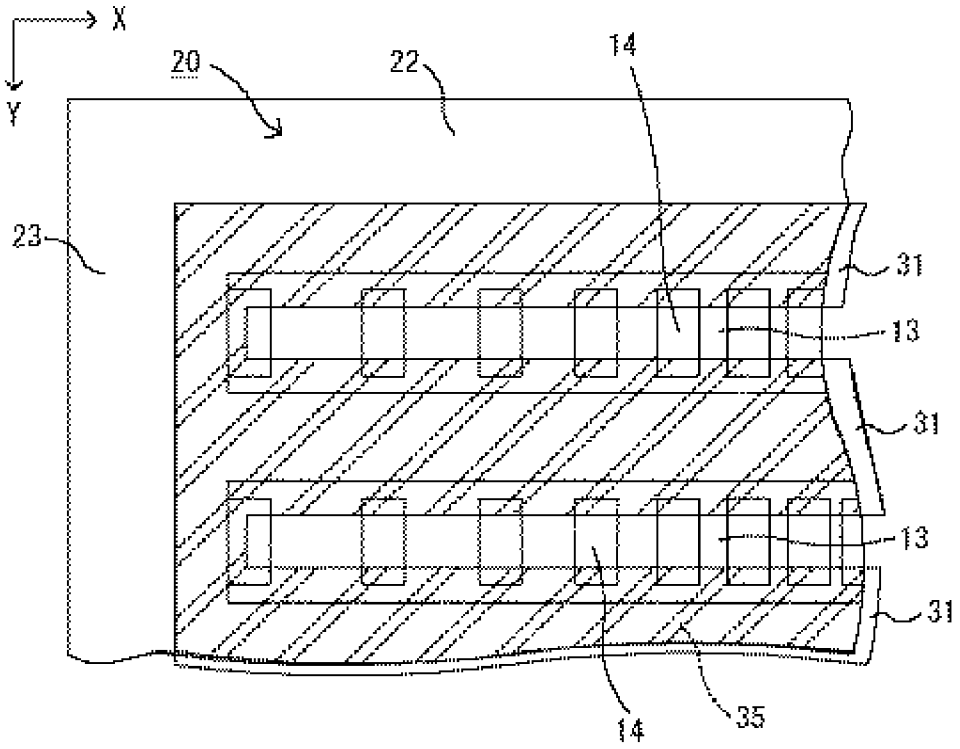


FIG. 12

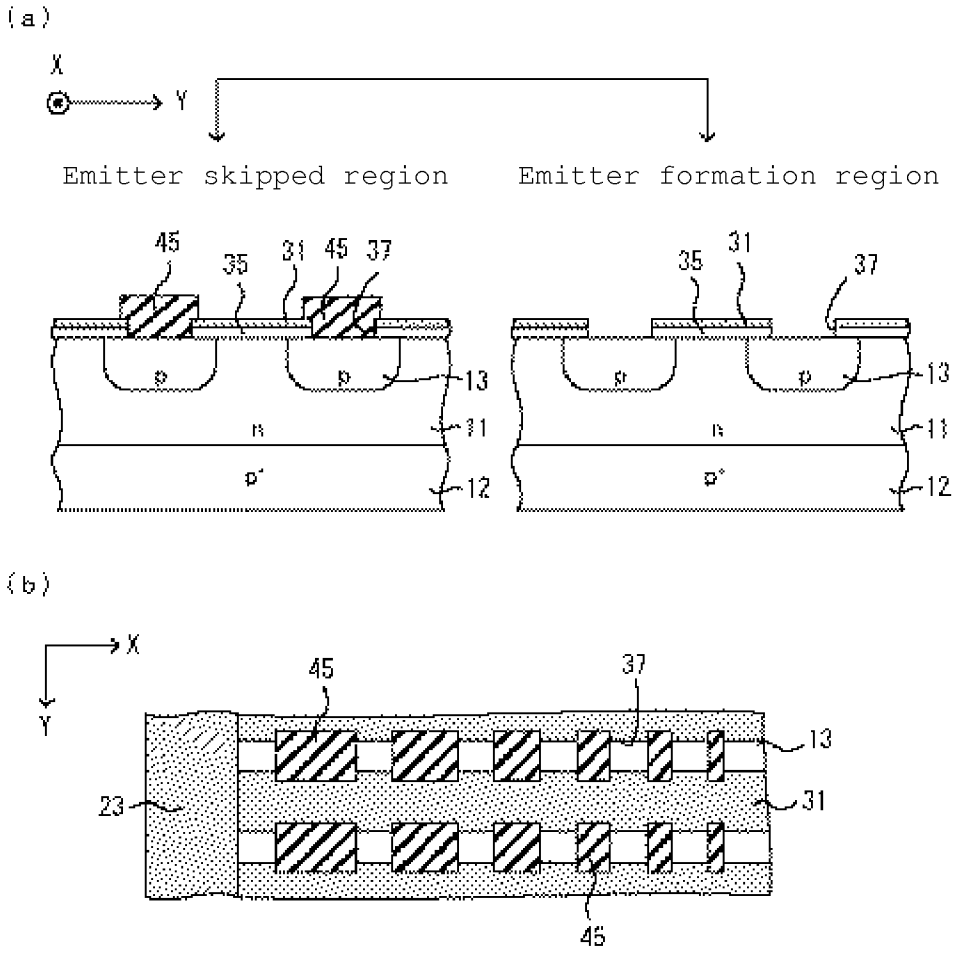

(a)
X
Y
Emitter skipped region
Emitter formation region
45
35
31
45
37
35
31
37
p
p
p
p
13
13
n
n
11
11
p+
p+
12
12
(b)
X
Y
45
37
13
23
31
45

FIG. 13

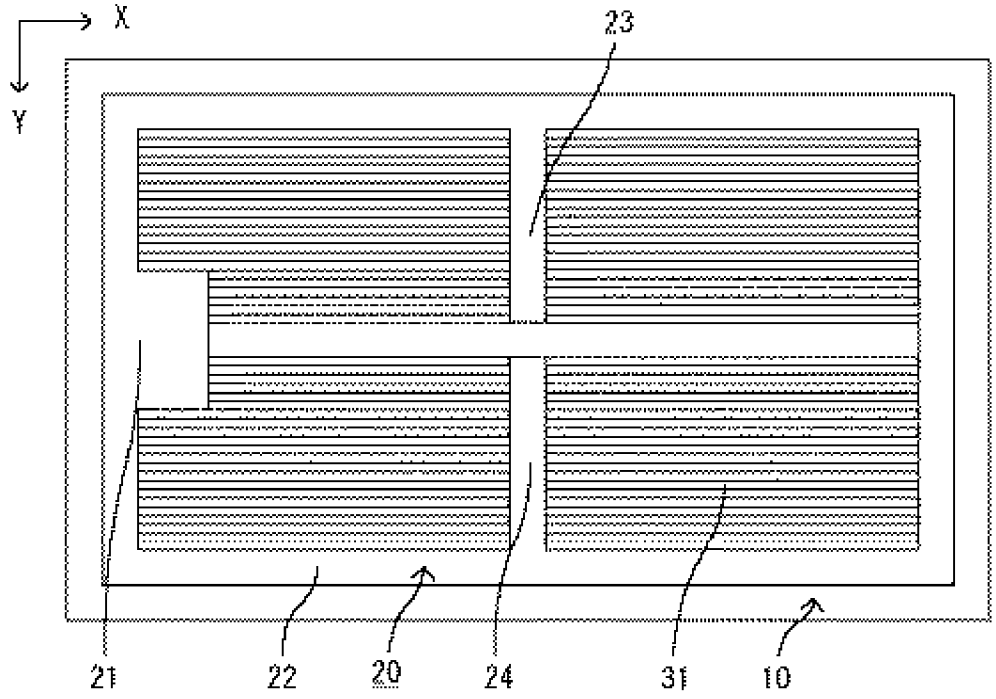


FIG. 14